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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/801,651

03/17/2004

Jeong-Hwan Yang

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09/01/2005

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EXAMINER

LINDSAY JR, WALTER LEE

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 09/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

ix

<b>Office Action Summary</b>	Application No. 10/801,651	Applicant(s) YANG, JEONG-HWAN	
	Examiner Walter L. Lindsay, Jr.	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 10-12, 14 and 16-31 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 10-12, 14, 16-19 and 26-31 is/are rejected.
- 7) ☒ Claim(s) 20-25 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

### **DETAILED ACTION**

This Office Action is in response an Amendment filed on 6/23/2005.

Currently, claims 10-12, 14 and 16-31 are pending.

#### ***Specification***

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

#### ***Claim Objections***

2. Claim 17 is objected to because of the following informalities: "suicide" in line 2 of claim 17 should be "silicide". Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 10-12, 14, 16 and 26-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Joshi et al. (U.S. Publication No. 2005/0017377 filed 7/21/2003).

Joshi shows the method as claimed in Figs. 4-8F and corresponding text as: the channel comprises an inner portion (24) and an outer portion (32) [0029]; the outer portion surrounds the inner portion [0029]; the inner portion and the outer portion have

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different lattice properties [0029]; and a gate (18) formed over the channel, wherein the gate surrounds at least a section of the channel on at least three sides [0031] (claim 10). Joshi teaches that the inner portion comprises silicon-germanium and the outer portion comprises silicon [0030] (claim 11). Joshi teaches that the outer portion surrounds the inner portion on at least three sides [0029] (claim 12). Joshi teaches that the gate is substantially perpendicular to the channel [0031] (claim 14). Joshi teaches that a gate oxide is formed between the channel and the gate [0031] (claim 16).

Joshi shows the method as claimed in Figs. 4-8F and corresponding text as: a substrate (20) [0028]; a channel having an inner portion (24) and an outer portion (32) formed on the substrate, wherein the inner portion and the outer portion have different lattice properties [0029]; and a gate (18) formed over the channel, and wherein the gate surrounds at least a section of the channel on at least three sides [0031] (claim 26). Joshi teaches that a gate oxide (33) is formed between the channel and the gate [0031] (claim 27). Joshi teaches that the gate is substantially perpendicular to the channel [0031] (claim 28).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. Claims 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (U.S. Publication No. 2005/0017377 filed 7/21/2003) in view of Yeo et al. (U.S. Publication No. 2004/0217420 filed 4/30/2003).

Joshi shows the method substantially as claimed and as described in the preceding paragraph.

Joshi lacks anticipation in not explicitly teaching that: 1) a metal silicide layer is formed on a top surface of the gate (claim 17).

Yeo teaches a semiconductor-on-insulator chip incorporating strained-channel. The gate electrode (160) may also be formed by the deposition of silicon and metal, followed by an anneal to form a metal silicide gate electrode material. An example, the silicide could be titanium silicide, nickel silicide or cobalt silicide [0075]. Therefore strain-induced mobility enhancement is another way to improve transistor performance in addition to device scaling [0014].

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Joshi, by forming a metal silicide on a top surface of the gate, as taught by Yeo, with the motivation that Yeo teaches that strain-induced mobility

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enhancement is another way to improve transistor performance in addition to device scaling.

8. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (U.S. Publication No. 2005/0017377 filed 7/21/2003).

Joshi shows the method substantially as claimed and as described in the preceding paragraph.

Joshi lacks anticipation in not explicitly teaching that: 1) the thickness of the inner portion is between 10 nm and 90 nm (claim 18); and 2) the thickness of the outer portion is between 10 nm and 100 nm (claim 19).

a. Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See *In re Aller*, Lacey and Hall (10 USPQ 233-237) It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

It would have been obvious to one of ordinary skill in the art at time the invention was made, to modify the teachings of Joshi, by optimizing the thickness of the layer,

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with the motivation that these would improve the structure and can be done through ordinary experimentation.

9. Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi et al. (U.S. Publication No. 2005/0017377 filed 7/21/2003) in view of Yeo et al. (U.S. Publication No. 2004/0217420 filed 4/30/2003).

Joshi shows the method as claimed in Figs. 4-8F and corresponding text as: a substrate (20) [0028]; a channel having an inner portion (24) and an outer portion (32) formed on the substrate, wherein the inner portion and the outer portion have different lattice properties [0029]; and a gate (18) formed over the channel, and wherein the gate surrounds at least a section of the channel on at least three sides [0031] (claim 29). Joshi teaches that the gate is substantially perpendicular to the channel [0031] (claim 30). Joshi teaches that a gate oxide (33) is formed between the channel and the gate [0031] (claim 31).

Joshi lacks anticipation in not explicitly teaching that: 1) a source region and a drain region to the channel (claim 29).

Yeo teaches a semiconductor-on-insulator chip incorporating strained-channel. Source and drain regions of the transistor device (150) are not shown. The channel current flows into and out of the page corresponding Fig. 3c with the source drain regions are connected to the channel [0047]. Therefore strain-induced mobility enhancement is another way to improve transistor performance in addition to device scaling [0014].

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It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Joshi, by forming a metal silicide on a top surface of the gate, as taught by Yeo, with the motivation that Yeo teaches that strain-induced mobility enhancement is another way to improve transistor performance in addition to device scaling.

***Allowable Subject Matter***

10. Claims 20-25 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...the outer portion includes a layer formed between the inner portion and the semiconductor substrate (claim 20).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.



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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.  
Examiner  
Art Unit 2812

WLL

August 29, 2005

